Specification Amendments

Please replace paragraph 0017 with the following rewritten paragraph:

0017 In addition, one or more layers of a high-K dielectric (e.g., dielectric constant greater than about 10), for example, tantalum pentaoxide (e.g., Ta_2O_5) may be used to form the gate dielectric 18. Other metal oxides such as, titanium oxides, (e.g., TiO_2), hafnium oxides (e.g., HfO_2), yttrium oxides (e.g., Y_2O_3), lanthanum oxides (e.g., La_2O_5), zirconium oxides (e.g., ZrO_2), and silicates and aluminates thereof may also be suitably used to form the gate dielectric 18, for example having an equivalent oxide thickness (EOT) of an SiO_2 gate dielectric, e.g., having a thickness of from about 50 Angstroms to about 200 Angstroms formed over a thermally grown interfacial oxide layer (not shown) formed over the silicon substrate 12. For example, atomic layer chemical vapor deposition (ALCVD) methods, followed by annealing treatments in oxygen, nitrogen and/or hydrogen may be used to ~~from~~ form a high-K gate dielectric layer stack. Further, other high dielectric constant materials, such as $BaSrTiO_3$ (BST), and $PbZrTiO_3$ (PZT) or other high-K materials, preferably having a dielectric constant greater than about 10, more preferably about 20, may be suitably used to form a high-K gate dielectric stack.

Please replace paragraph 0024 with the following rewritten paragraph:

0024 Referring to Figure 1F, a conventional salicide (self aligned silicide) formation process is then carried out by first removing material layers overlying the silicon substrate 12 (e.g., oxide portions), followed by deposition of a metal, for example Ti or Co and a silicidation process to form salicides e.g., $TiSi_2$ or $CoSi_2$, 28A, 28B, and 28C respectively aligned over P+ doped region 24A, the pass transistor 22A, and the storage capacitor 22B. Advantageously the unetched spacer dielectric layer portion 26B operates to prevent salicide formation over the P- doped region 24[[A]]B. Conventional process are then carried out to form appropriate conductive interconnects (not shown), for example providing a respective conductive interconnects to electrically connect to e.g., salicide portion 28A (bit line) of P+ doped region 24A, salicide portion 28B (word line) of pass transistor 22A, and salicide portion 28C of storage capacitor 22B.